27. (amended) The display of claim 20 wherein a number of ILLUMINATE periods and LOAD periods that are used to illuminate said electroluminescent cell during a frame [period]time is equivalent to a number of bits [in said data signal]used to define a number of levels of gray.

REMARKS

Objections

A. 35 U.S.C. § 132

The Examiner has objected to the amendment of January 22, 1998 under 35 U.S.C. § 132 because the amendment introduces new matter into the disclosure. The applicants disagree.

FIGs. 7 and 8 were introduced in support of, for example, independent claims 8, 14, 20 and 30 at the insistence of the Examiner to provide a depiction of each and every feature of these new claims in the figures as required under 37 C.F.R. 1.83(a). However, the applicants have now amended these claims to clearly rely upon the text of the specification, as filed, such that FIGs. 7 and 8 are not necessary to understand the invention as it is now claimed. Although the applicants did not believe that such drawings were necessary to understanding and practicing the invention under 37 CFR 1.81(a), the prior amendment added drawings to fulfill the § 1.83(a) requirement as requested by the Examiner and expedite allowance of this patent application. The drawings, as discussed below, were prepared by the applicant's undersigned attorney using the specification of the application as his sole source of information. As such, FIGs. 7 and 8 are derived directly from the specification, as filed, and do not contain new matter.

1. Objection of FIG. 7

As to FIG. 7, this figure depicts the various signals that exist within the electroluminescent (EL) cell control circuit. These signals are explicitly described in the text of the specification and the applicant's attorney merely used the words of the specification to produce the figure. Specifically, the first (top) portion of the figure depicts a frame time being subdivided into a number of LOAD and ILLUMINATE periods as described on page 4, lines 12-16.

The next portion of FIG. 7 depicts a relative comparison of a data signal and a ramp control signal (analog signal) within a frame period. The use of this signal is explicitly described at page 3, line 61 to page 4, line 2 where the ramp control signal varies from "5V to -5V during the field", i.e., the ramp extends over one frame time and the storage capacitor "stores -1.5V" representing a data value. As described in the specification, in this example, the transistor conducts current during 32 of the 128 ILLUMINATE periods within a frame period (i.e., approximately, 25% brightness). The last (bottom) graph of FIG. 7 depicts this current being conducted during some of the ILLUMINATE periods (e.g., 32) and not conducting during other ILLUMINATE periods (e.g., 96). Thus, the first, second, and fourth graphs explicitly depict the text of the specification that describes the operation of grayscale pixel control using an analog control signal as described with respect to the example on page 3, line 61 et seq. and elsewhere in the specification.

On page 3, lines 62-64 the specification states that the variable voltage applied to the data line over a frame time is a "ramp of voltage" or "a step function in voltage". This is what is depicted in the third time graph of FIG. 7, a step waveform that generally follows the slope of the ramp waveform.

Clearly, the text of the specification, as filed, supports the various graphs of FIG. 7. Consequently, FIG. 7 does not add any new matter to the specification as filed. As such, the

applicant believes the objection to FIG. 7 is inappropriate and respectfully requests that the objection be withdrawn.

2. Objection of FIG. 8

Similarly to the discussion above, FIG. 8 also contains various signal graphs that depict signals for digital pixel control that were explicitly described in the specification, as filed.

Specifically, on page 4, lines 12-16, the frame time is described as being subdivided into a number of LOAD and ILLUMINATE periods. This period arrangement is depicted in the first (top) graph of FIG. 8.

On page 4, lines 16-19, the specification states that during the LOAD periods data is loaded into the pixel circuitry based upon the significance of each data bit, i.e., the least significant bit (LSB) is loaded during the first LOAD period, the "next most significant bit" is loaded during the second LOAD period and so on. This bit significant loading is what is depicted in the second (middle) graph of FIG. 8. Furthermore, the applicant has amended FIG. 8 to address the Examiner's concern that the MSB and LSB were not labeled on the graph. The applicant's proposed amendment is indicated in red ink on the attached figure.

The last (bottom) graph of FIG. 8 depicts the pulsed current that is conducted during the ILLUMINATE periods with respect to the significance of each bit. As described on page 4, lines 19-30 the LSB corresponds to one current pulse, the next significant bit corresponds to two current pulses, and so on.

Clearly, FIG. 8 is merely a depiction of the content of the specification, as filed, and does not contain any new matter. Consequently, the applicant believes that the objection to FIG. 8 is inappropriate and respectfully requests that the objection be withdrawn.

3. Objection of the claims 8-12 14 and 20.

The Examiner specifically objected to claims 8, 9, 10, 11, 12, 14 and 20 as not being supported by the specification, as filed. In response, the applicant has amended these claims and believes that these claims are now fully supported by the specification.

The Examiner objected to claim 8, lines 13-18 as not supported by the specification as filed. The objected to portion of claim 8 has been amended to recite:

> "varying, during each of said ILLUMINATE periods, a voltage on the data line to selectively illuminate said electroluminescent cell in response to said voltage and said stored data."

This clause recites the process described in the specification at page 3, lines 15 to page 4, line 17 (analog control) and again at page 4, lines 12-22 (digital control). In each instance, a data line signal (data) is stored on the gate of transistor 80 in the pixel circuit, e.g., -1.5V, during a LOAD period to activate the pixel. See, for example, page 3, lines 13-25. Then, as described on page 3, lines 25-31, during each ILLUMINATE period, a voltage is applied to the data line and varied to selectively illuminate the electroluminescent cell. This portion of the specification recites all the limitations of the quoted clause of claim 8, as amended. As such, the specification fully supports claim 8, as amended, and the objection should be withdrawn.

As for claim 9, the applicants have canceled claim 9.

As for claim 10, the applicants have amended claim 10 to recite the terminology used in the specification. As such, claim 10 now recites "a voltage on said data line is a linear ramp." This recitation finds support on page 3, lines 58-64 which state that the data line "voltage variation can be a linear ramp of the voltage." The recitation of claim 10 is nearly identical to the

recitation of the data line voltage definition in the specification. As such, the specification supports the limitation recited in claim 10.

As for claim 11, the applicants have amended claim 11 to recite the substantive terminology used in the specification. As such, claim 11 now recites "a voltage on said data line is a step function." Page 3, lines 58-64 state that the data line "voltage variation can be ... a step function in voltage." The recitation of claim 10 is nearly identical to the recitation of the data line voltage definition in the specification. As such, the specification supports the limitation recited in claim 11.

As for claim 12, the applicant has amended claim 12 to recite that "during each ILLUMINATE period, a high voltage source applies one or more pulses to said circuit and, in response to said voltage, said pulses are applied to said electroluminescent cell." The specification discloses on page 4, lines 19-21 a "high voltage source" that emits a number of pulses during the ILLUMINATION periods. On page 2, lines 22-48 of the applicant's specification, the details of the interconnection of the high voltage source to the pixel circuitry is delineated and how the high voltage source produces current that is coupled through pixel circuitry to the electroluminescent cell. As such, claim 12 is now fully supported by the specification and the applicant respectfully requests the objection of claim 12 to be withdrawn.

In claims 14 and 20, the Examiner objected to the limitations "dividing said frame period into a plurality of LOAD periods and a plurality of ILLUMINATE periods, where each LOAD period is followed by an ILLUMINATE period" and "during each of said LOAD periods ... data signal stored; during each of said ILLUMINATE periods, ... electroluminescent cell" are not supported by the specification as filed. In response, the applicant has substantially amended claims 14 and 20 to reiterate the terminology of the specification. As such, the recitations of claims 14 and 20 are now fully supported by the specification, as filed. Specifically, the disclosures of subdividing a frame time

into a number of LOAD and ILLUMINATE periods, referred to in the specification as sub-frames, are numerous and reiterated throughout the specifications. See for example, page 3, lines 15-16, where a "frame time" is sub-divided into "separate LOAD periods and ILLUMINATE periods". Thus, a single frame time is subdivided into sub-periods. Note that the LOAD and ILLUMINATE periods are both recited as plural terms indicating a plurality of each period within a frame time. On page 4, line 30-34, the specification states that the procedure is equivalent "to dividing a frame into a number of sub-frames", i.e., a number of "LOAD/ILLUMINATE periods" (page 4,line 14). To closely follow the recitation of the specification, the claims have been amended to recite that the frame time is subdivided into a number of LOAD and ILLUMIINATE periods. As such, the objected clause is no longer recited in the claims and the new recitation is clearly supported by the specification.

The second objected clause recites the specific operation of the gray-scale control of the circuit. This operation is clearly recited in the example at page 3, line 64 to page 4, line 2 to support claim 14 (as discussed above with respect to claim 8) and at page 2, lines 35 to 48 to support claim 20 where the specification describes the detailed operation of loading the dual transistor circuit with data during a LOAD period and then activating the EL cell during an ILLUMINATE period in response to the loaded data. As such, the recited limitations of claims 14 and 20 are clearly described in the specification. Therefore, the applicant respectfully requests that the objection to these claims be withdrawn.

Rejections

A. 35 U.S.C. §112 - claims 8-16, 18-20, 25, and 27-29

The Examiner has rejected claims 8-16, 18-20, 25, and 27-29 under 35 U.S.C. §112, first paragraph, as containing subject

matter which was not adequately described in the specification. This rejection is respectfully traversed.

The Examiner's rejection is based upon the reasoning stated above in objecting to the specification and claims. For the reasons stated above, the applicant believes all the objections are overcome and that the specification and drawings do not contain any new matter. As such, the claims of the application are fully supported by the specification, as filed. Therefore, the applicant respectfully requests that this rejection be withdrawn.

Conclusion

The applicant submits that all of these claims now fully satisfy the requirements of 35 U.S.C. § 112. Consequently, the applicants believe that all these claims are presently in condition for allowance. Accordingly, both reconsideration of this application and its swift passage to issue are earnestly solicited.

If, however, the Examiner believes that there are any unresolved issues requiring adverse final action in any of the claims now pending in the application, it is requested that the Examiner telephone Mr. Raymond R. Moser Jr., Esq. at (732) 530-9404 so that appropriate arrangements can be made for resolving such issues as expeditiously as possible.

Respectfully submitted,

12-28-98

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I hereby certify that this patent application and related papers is being deposited with the United States Postal Service "Express Mail Post Office to Addressee" service under 37 CFR 1.10 on the date indicated above and is addressed to the Assistant Commissioner for Patents, Washington, D.C. 20231.

Kathleen Faushan
Signature of person mailing paper or fee

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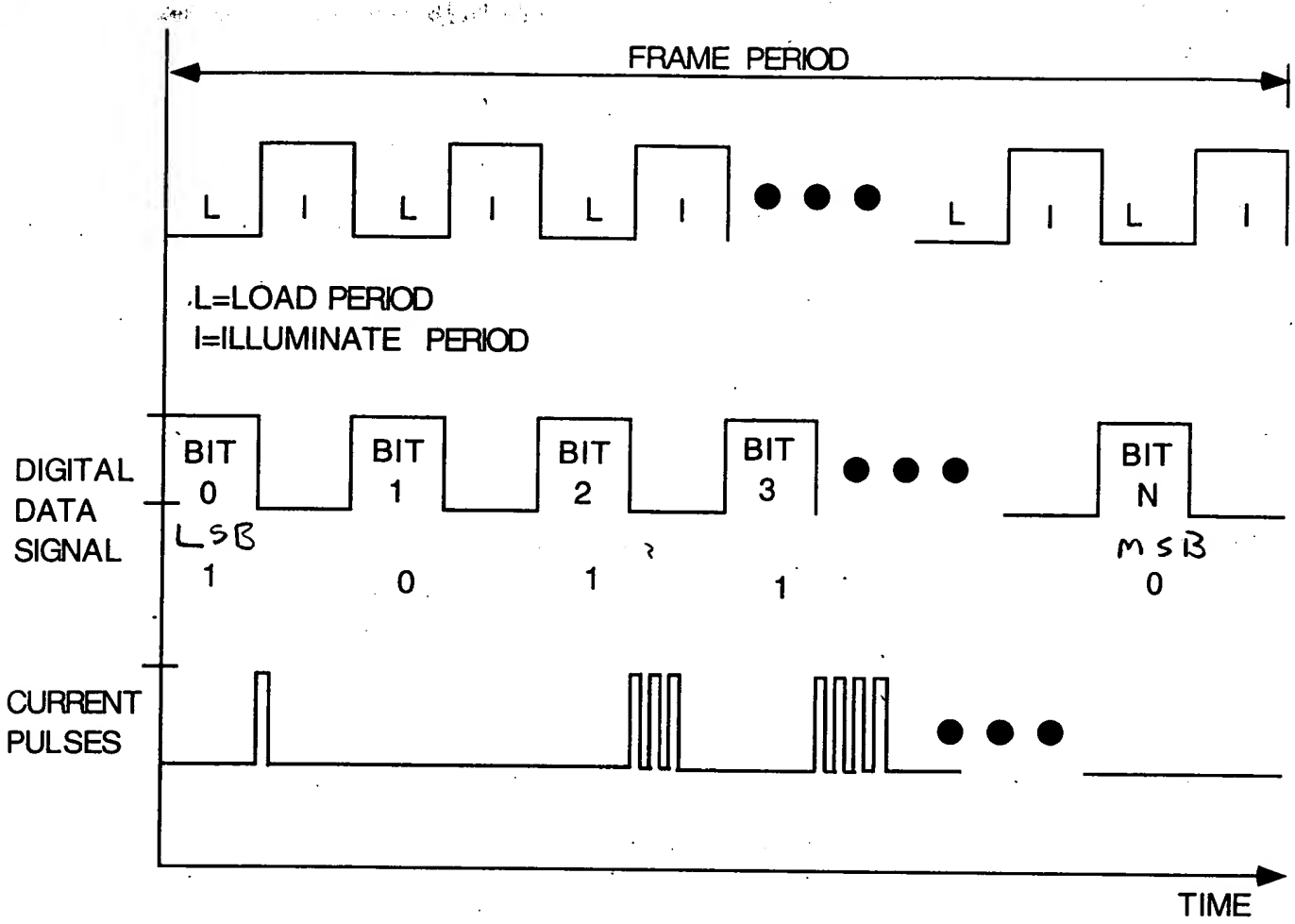
FRAME PERIOD
L
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L=LOAD PERIOD
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DIGITAL DATA SIGNAL
BIT 0
BIT 1
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BIT 3
BIT N
LSB
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1
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CURRENT PULSES
TIME

FIG. 8

NEW